CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device, comprising:

a main array including a plurality of columns of CAM cells;

a spare column of CAM cells to functionally replace a defective column of CAM cells in the main array; and

means for shifting data corresponding to the defective column and data corresponding to all subsequent columns in the main array to corresponding adjacent non-defective columns in the main array and the spare column.

2. The CAM device of Claim 1, wherein the means for shifting comprises:

means for steering data from the defective column to a next column in the main array;

means for steering data from each column in the main array subsequent to the defective column to an adjacent column in the main array; and

means for steering data from a last column in the main array to the spare column.

3. The CAM device of Claim 2, further comprising:

means for decoding the column address to generate a plurality of column control signals.

4. The CAM device of Claim 3, further comprising:

means for masking the defective column during a compare operation in response to the column control signals.

5. The CAM device of Claim 1, wherein the means for

shifting comprises:

a plurality of multiplexers, each corresponding to a different column in the main array and each having a first input to receive data for the corresponding column, a second input to receive data for an adjacent column, a control terminal to receive a corresponding column control signal, and an output coupled to the corresponding column.

6. The CAM device of Claim 5, wherein the adjacent column comprises a previous column in the main array.

7. The CAM device of Claim 5, further comprising:

a column decoder for generating the column control signals in response to a defective column address.

8. The CAM device of Claim 7, wherein each column control signal indicates whether a corresponding column is defective.

9. The CAM device of Claim 1, wherein the means for shifting comprises:

a plurality of multiplexers, each corresponding to a different column and each having a first input coupled to the corresponding column, a second input coupled to an adjacent column, a control terminal to receive a corresponding column control signal, and an output.

10. The CAM device of Claim 9, wherein the adjacent column comprises a next column.

11. The CAM device of Claim 10, further comprising:

a column decoder for generating the column control

signals in response to a defective column address.

12. The CAM device of Claim 11, wherein each column control signal indicates whether a corresponding column is defective.

13. The CAM device of Claim 1, wherein each column of CAM cells in the main array is coupled to a bit line pair and a comparand line pair and the spare column is coupled to a spare bit line pair and a spare comparand line pair.

14. The CAM device of Claim 1, wherein the spare column comprises a plurality of spare columns.

15. A content addressable memory (CAM) device, comprising:

a main array including a plurality of columns of CAM cells, each column having an input to selectively receive one of two corresponding adjacent bits of a data word in response to a corresponding column control signal; and

a spare column of CAM cells having an input to selectively receive a last bit of the data word in response to a spare column control signal.

16. The CAM device of Claim 15, further comprising:

a column decoder to generate the column control signals in response to a defective column address.

17. The CAM device of Claim 16, wherein each column control signal indicates whether the corresponding column is defective.

18. The CAM device of Claim 15, wherein each column further comprises:

a multiplexer having inputs to receive the corresponding adjacent bits of the data word, a control terminal to receive the corresponding column control signal, and an output coupled to the input of the column.

19. The CAM device of Claim 18, wherein the multiplexers shift the data bits corresponding to the defective column and to all subsequent columns in the main array to corresponding next columns in the main array and to the spare column.

20. A content addressable memory (CAM) device, comprising:

a main array including a plurality of columns of CAM cells;

a spare column of CAM cells; and

a plurality of multiplexers, each having a first input coupled to a corresponding column, a second input coupled to a next column, a control terminal to receive a corresponding column control signal, and an output.

21. The CAM device of Claim 20, wherein the output of multiplexer selectively outputs either a data bit from the corresponding column or a data bit from the next column in response to the corresponding column control signal.

22. The CAM device of Claim 20, further comprising:

a column decoder to generate the column control signals in response to a defective column address.

23. The CAM device of Claim 22, wherein each column control signal indicates whether the corresponding column is defective.